Complete Single Supply 12-Bit Voltage Output DAC in SO-8

FEATURES

- **8-Pin SO Package**
- **Buffered Voltage Output**
- **Built-In 2.048V Reference**
- 500µV/LSB with 2.048V Full Scale
- 1/2 LSB Max DNL Error
- Guaranteed 12-Bit Monotonic
- Three-Wire Cascadable Serial Interface
- Wide Single Supply Range: V_{CC} = 4.75V to 15.75V
- Low Power: I_{CC} Typ = 350µA with 5V Supply

APPLICATIONS

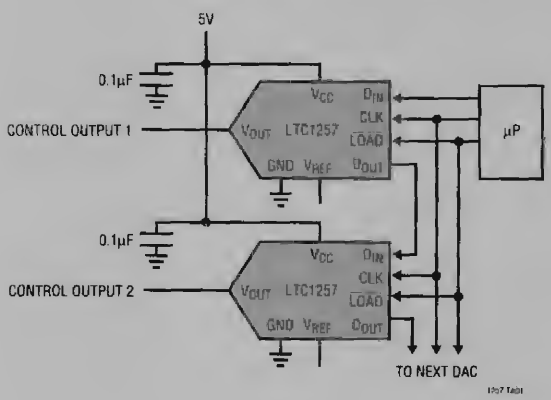
- Digital Offset/Gain Adjustment
- Industrial Process Control
- Automatic Test Equipment

DESCRIPTION

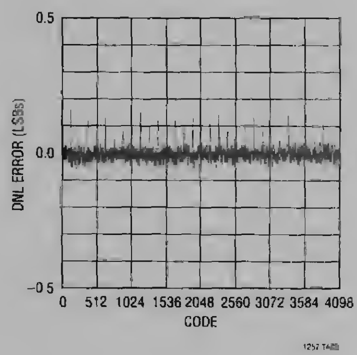
The LTC1257 is a complete single supply, 12-bit voltage output D/A converter (DAC) in an SO-8 package. The LTC1257 includes an output buffer amplifier, 2.048V voltage reference and an easy to use three-wire cascadable serial interface. An external reference can be used to override the internal reference and extend the output voltage range to 12V. The power supply current is a low 350µA when operating from a 5V supply, making the LTC1257 ideal for battery-powered applications. The space-saving 8-pin SO package and operation with no external components provide the smallest 12-bit D/A system available.

TYPICAL APPLICATION

Daisy Chained Control Outputs



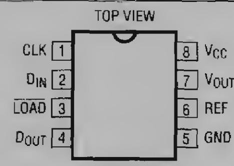
Differential Nonlinearity vs Input Code



ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .... −0.5V to 16.5V
TTL Input Voltage .... −0.5V to V_{CC} + 0.5V
V_{OUT} .... −0.5V to V_{CC} + 0.5V
REF .... −0.5V to V_{CC} + 0.5V
Operating Temperature Range
  LTC1257C .... 0°C to 70°C
  LTC1257I .... −40°C to 85°C
Maximum Junction Temperature
  Plastic Package .... −65°C to 125°C
Storage Temperature Range .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec)................ 300°C

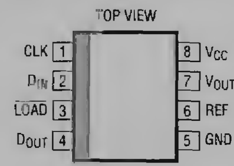
PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PLASTIC DIP
T_{JMAX} = 125°C, θ_{JA} = 100°C/W

ORDER PART NUMBER

LTC1257CN8
LTC1257IN8



S8 PACKAGE
8-LEAD PLASTIC SOIC
T_{JMAX} = 125°C, θ_{JA} = 150°C/W

LTC1257CS8
LTC1257IS8

S8 PART MARKING
1257C
1257I

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{CC} = 4.75V to 15.75V, internal or external reference (2.475V ≤ V_{REF} ≤ V_{CC} − 2.7V), I_{OUT} ≤ 2mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DAC							
	Resolution		●	12			Bits
DNL	Differential Nonlinearity	Guaranteed Monotonic	●			±0.5	LSB
INL	Integral Nonlinearity	LTC1257C	●			±3.5	LSB
		LTC1257I	●			±4.0	LSB
OFF	Offset Error	When Using Internal Reference, LTC1257C	●			±8	LSB
		When Using Internal Reference, LTC1257I	●			±10	LSB
		When Using External Reference, LTC1257C	●			±4	mV
		When Using External Reference, LTC1257I	●			±5	mV
OFF_{TC}	Offset Error Tempco	When Using Internal Reference (Note 1)	●		±0.02	±0.066	LSB/°C
		When Using External Reference (Note 1)	●		±15	±30	μV/°C
FSE	Full-Scale Error		●		0.5	±2	LSB
FSE_{TC}	Full-Scale Error Tempco	(Note 1)	●		±0.01	±0.02	LSB/°C
Reference							
	Reference Output Voltage	I_{OUT} = 0, LTC1257C	●	2.028	2.048	2.068	V
		I_{OUT} = 0, LTC1257I	●	2.018		2.078	V
	Reference Output Tempco	I_{OUT} = 0	●		±0.06		LSB/°C
	Reference Line Regulation	I_{OUT} = 0, LTC1257C	●			±0.4	LSB/V
		I_{OUT} = 0, LTC1257I	●			±0.7	LSB/V
	Reference Load Regulation	0 ≤ I_{OUT} ≤ 100μA	●			±1	LSB
	Reference Input Range	V_{CC} > V_{REF} + 2.7V	●	2.475		12	V
	Reference Input Resistance		●	8	14	18	kΩ
	Reference Input Capacitance	(Note 1)			15		pF
	Short-Circuit Current	V_{OUT} Shorted to GND	●			90	mA

ELECTRICAL CHARACTERISTICS

V_{CC} = 4.75V to 15.75V, internal or external reference (2.475V ≤ V_{REF} ≤ V_{CC} – 2.7V), I_{OUT} ≤ 2mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply							
V_{CC}	Positive Supply Voltage	For Specified Performance	●	4.75		15.75	V
I_{CC}	Supply Current	4.75V ≤ V_{CC} ≤ 5.25V 4.75V ≤ V_{CC} ≤ 15.75V	● ●		350 800	600 1500	μA μA
Op Amp DC Performance							
	Short-Circuit Current Low	V_{OUT} Shorted to GND	●			60	mA
	Short-Circuit Current High	V_{OUT} Shorted to V_{CC}	●			60	mA
	Output Impedance to GND	Input Code = 0	●		150	300	Ω
AC Performance							
	Voltage Output Slew Rate	5kΩ in Parallel with 100pF	●	1.0			V/μs
	Voltage Output Settling Time	To ±1/2LSB, 5kΩ in Parallel with 100pF	●			6	μs
	Digital Feedthrough	(Notes 1,2)			50		nV/s
Digital I/O							
V_{IH}	Digital Input High Voltage		●	2.4			V
V_{IL}	Digital Input Low Voltage		●			0.8	V
V_{OH}	Digital Output High Voltage	I_{OUT} = –1mA, D_{OUT} Only	●	V_{CC} – 1			V
V_{OL}	Digital Output Low Voltage	I_{OUT} = 1mA, D_{OUT} Only	●	0.4			V
I_{LEAK}	Digital Input Leakage	V_{IN} = GND to V_{CC}	●			±10	μA
C_{IN}	Digital Input Capacitance	(Note 1)	●			10	pF
Switching (Note 1)							
t1	D_{IN} Valid to CLK Setup		●	150			ns
t2	D_{IN} Valid to CLK Hold		●	0			ns
t3	CLK High Time		●	350			ns
t4	CLK Low Time		●	350			ns
t5	$\overline{\text{LOAD}}$ Pulse Width		●	150			ns
t6	LSB CLK to $\overline{\text{LOAD}}$		●	0			ns
t7	$\overline{\text{LOAD}}$ High to CLK		●	0			ns
t8	D_{OUT} Output Delay	C_{LOAD} = 15pF	●			150	ns
f_{CLK}	Maximum Clock Frequency					1.4	MHz

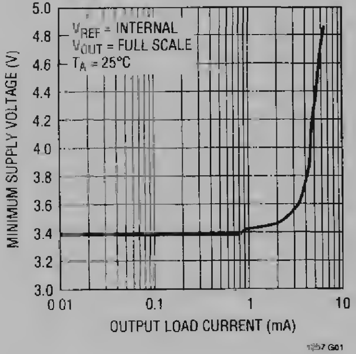
The ● denotes specifications which apply over the full operating temperature range.

Note 1: Guaranteed by design; not subject to test.

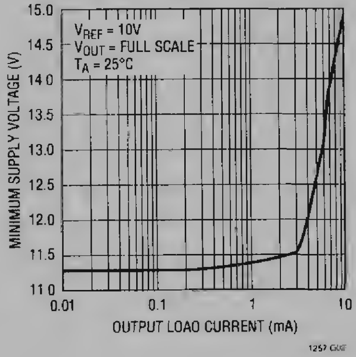
Note 2: DAC switched from all 1s to all 0s, and all 0s to all 1s code.

TYPICAL PERFORMANCE CHARACTERISTICS

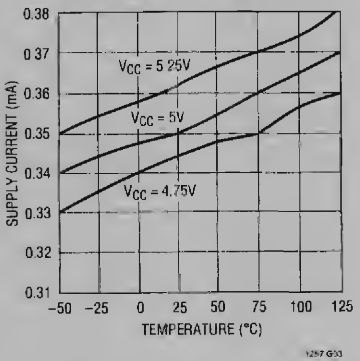
Minimum Supply Voltage vs Load Current #1



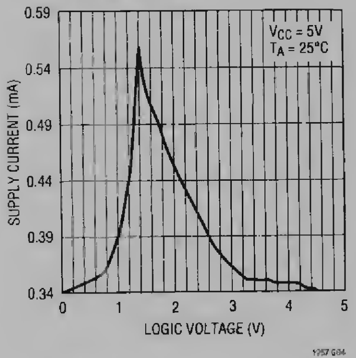
Minimum Supply Voltage vs Load Current #2



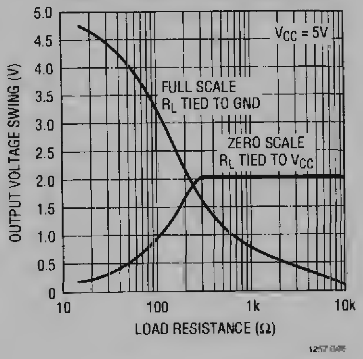
Supply Current vs Temperature



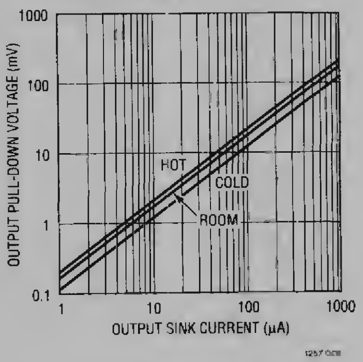
Supply Current vs Logic Input Voltage



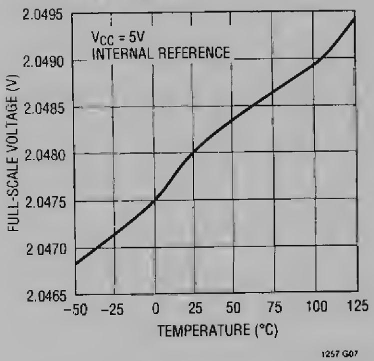
Output Swing vs Load Resistance



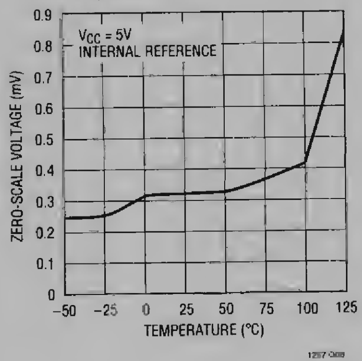
Pull-Down Voltage vs Output Sink Current Capability



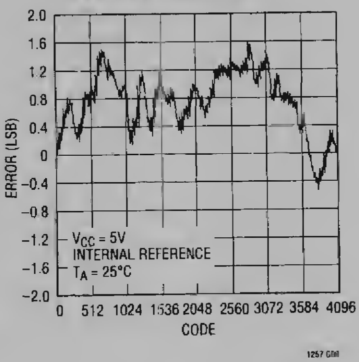
Full-Scale Voltage vs Temperature



Zero-Scale Voltage vs Temperature

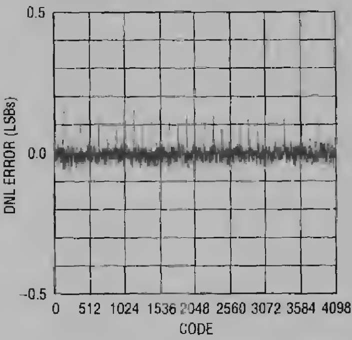


Integral Nonlinearity (INL)

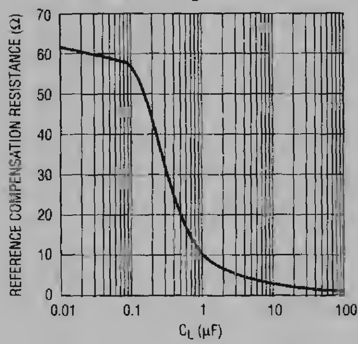


TYPICAL PERFORMANCE CHARACTERISTICS

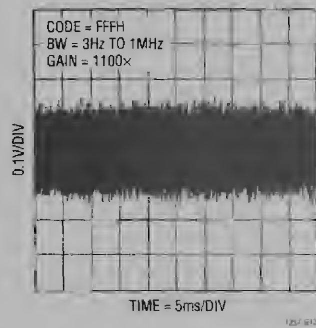
Differential Nonlinearity (DNL)



Reference Compensation Resistance vs C_L



Broadband Noise



PIN FUNCTIONS

CLK: The TTL level input for the serial interface clock.

D_{IN}: The TTL level input for the serial interface data. Data on the D_{IN} pin is latched into the shift register on the rising edge of the serial clock.

$\overline{\text{LOAD}}$: The TTL level input for the serial interface load control. Data is loaded from the shift register into the DAC register, thus updating the DAC output when $\overline{\text{LOAD}}$ is pulled low. The DAC register is transparent as long as $\overline{\text{LOAD}}$ is held low.

D_{OUT}: The output of the shift register which becomes valid on the rising edge of the serial clock. The D_{OUT} pin is driven from GND to V_{CC} by an internal CMOS inverter. Multiple LTC1257s may be cascaded by connecting the D_{OUT} pin to the D_{IN} pin of the next chip.

GND: Ground.

REF: The output of the 2.048V reference and the input to the DAC resistor ladder. An external reference with voltage from 2.475V to V_{CC} – 2.7V may be used to override the internal reference.

V_{OUT}: The buffered DAC output is capable of sourcing 2mA over temperature while pulling within 2.7V of V_{CC}. The output will pull to ground through an internal 200Ω equivalent resistance.

V_{CC}: The positive supply input. $4.75V \le V_{CC} \le 15.75V$. Requires a bypass capacitor to ground.

DEFINITIONS

LSB: The least significant bit or the ideal voltage difference between two successive codes.

$LSB = (V_{FS} - V_{OS})/2^n - 1$

n = The number of digital input bits

V_{OS} = The zero code error or offset of the DAC

V_{FS} = The full-scale output voltage of the DAC measured when all bits are set to 1

Resolution: The resolution is the number of DAC output states (2^n) that divide the full-scale range. The resolution does not imply linearity.

INL: End-point integral nonlinearity is the maximum deviation from a straight line passing through the end-points of the DAC transfer curve. Because the part operates from a single supply and the output cannot go below ground, the linearity is measured between full-scale and the first code that guarantees a positive output. The INL error at a given input code is calculated as follows:

$INL = (V_{OUT} - V_{IDEAL})/LSB$

$V_{IDEAL} = (Code \times LSB) + V_{OS}$

V_{OUT} = The output voltage of the DAC measured at the given input code

DNL: Differential nonlinearity is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. The DNL error between any two codes is calculated as follows:

$DNL = (\Delta V_{OUT} - LSB)/LSB$

ΔV_{OUT} = The measured voltage difference between two adjacent codes

Offset Error: The theoretical voltage at the output when the DAC is loaded with all zeros. The output amplifier can have a true negative offset, but because the part is operated from a single supply, the output cannot go below ground. If the offset is negative, the output will remain near 0V resulting in the transfer curve shown in Figure 1.

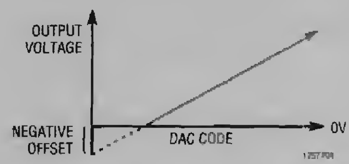


Figure 1. Effect of Negative Offset

The offset of the part is measured at the first code that produces an output voltage 0.5LSB greater than the previous code:

$V_{OS} = V_{OUT} - [(Code \times V_{FS})/(2^n - 1)]$

Full-Scale Error: Full-scale error is the difference between the ideal and measured DAC output voltages with all bits set to one (Code = 4095). The full-scale error includes the offset error and is calculated as follows:

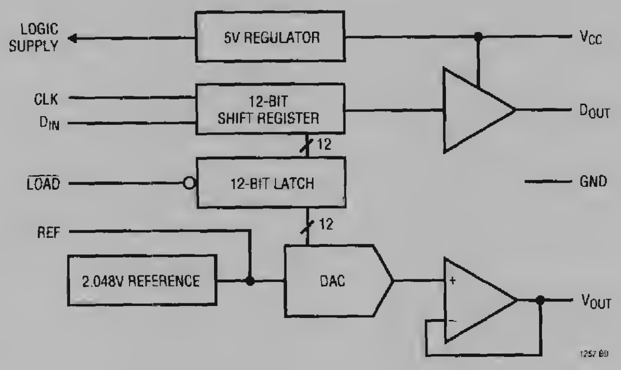
$FSE = (V_{OUT} - V_{IDEAL})/LSB$

$V_{IDEAL} = [V_{REF} \times (1 - 2^{-n})] - V_{OS}$

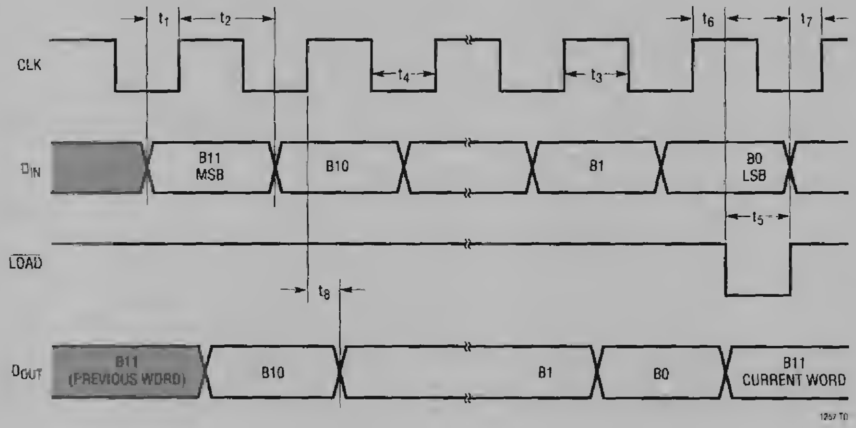
V_{REF} = The reference voltage, either internal or external

Digital Feedthrough: The glitch that appears at the analog output caused by AC coupling from the digital inputs when they change state. The area of the glitch is specified in nV × sec.

BLOCK DIAGRAM



TIMING DIAGRAM



OPERATION

Serial Interface

The data on the D_{IN} input is loaded into the shift register on the rising edge of the clock. The MSB is loaded first and the LSB last. The DAC register loads the data from the shift register when $\overline{LOAD}$ is pulled low, and remains transparent until $\overline{LOAD}$ is pulled high and the data is latched.

An internal 5V regulator provides the supply for the digital logic. By limiting the internal digital signal swings to 5V, digital noise is reduced. The buffered output of the 12-bit shift register is available on the D_{OUT} pin which will swing from GND to V_{CC}.

Multiple LTC1257s may be daisy chained together by connecting the D_{OUT} pin to the D_{IN} pin of the next chip, while the clock and load signals remain common to all chips in the daisy chain. The serial data is clocked to all of the chips, then the $\overline{LOAD}$ signal is pulled low to update all of them simultaneously. The maximum clocking rate is 1.4MHz.

Reference

The LTC1257 includes an internal 2.048V reference, making 1LSB equal to 500µV. The internal reference output is turned off when the pin is forced above the reference voltage, allowing an external reference to be connected to the reference pin. The external reference must be greater than 2.475V and less than V_{CC} – 2.7V, and be capable of driving the 10k minimum DAC resistor ladder.

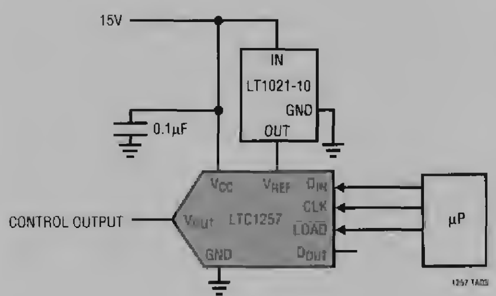
If the reference output is driving a large capacitive load, a series resistor must be added to insure stability. For any capacitive load greater than 1µF, a 10Ω series resistor will suffice.

Voltage Output

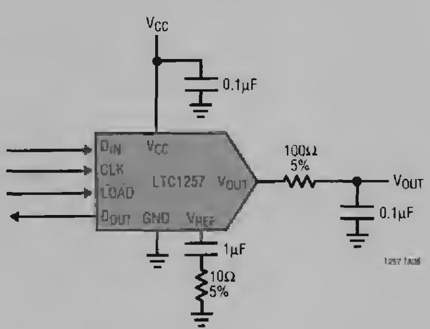
The LTC1257 voltage output is able to pull within 2.7V of V_{CC} while sourcing 2mA. A internal NMOS transistor with a 200Ω equivalent impedance pulls the output to ground. The output is protected against short circuits and is able to drive up to a 500pF capacitive load without oscillation. If digital noise on the output causes a problem, a simple 100Ω, 0.1µF RC circuit can be used to filter the noise.

TYPICAL APPLICATIONS

DAC with External Reference

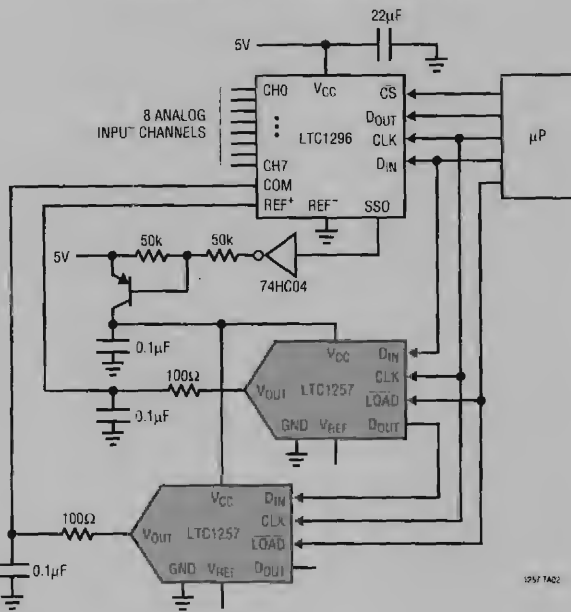


Filtering V_{REF} and V_{OUT}

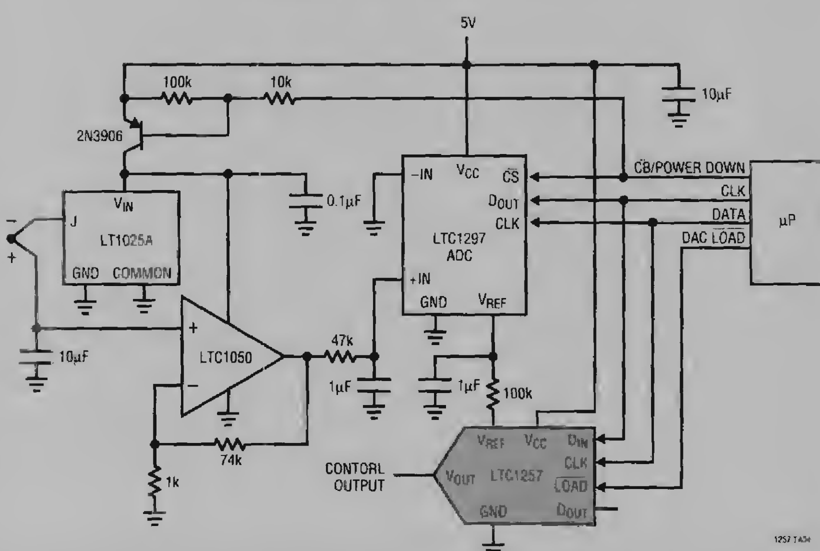


TYPICAL APPLICATIONS

Auto Ranging 8-Channel ADC with Shutdown

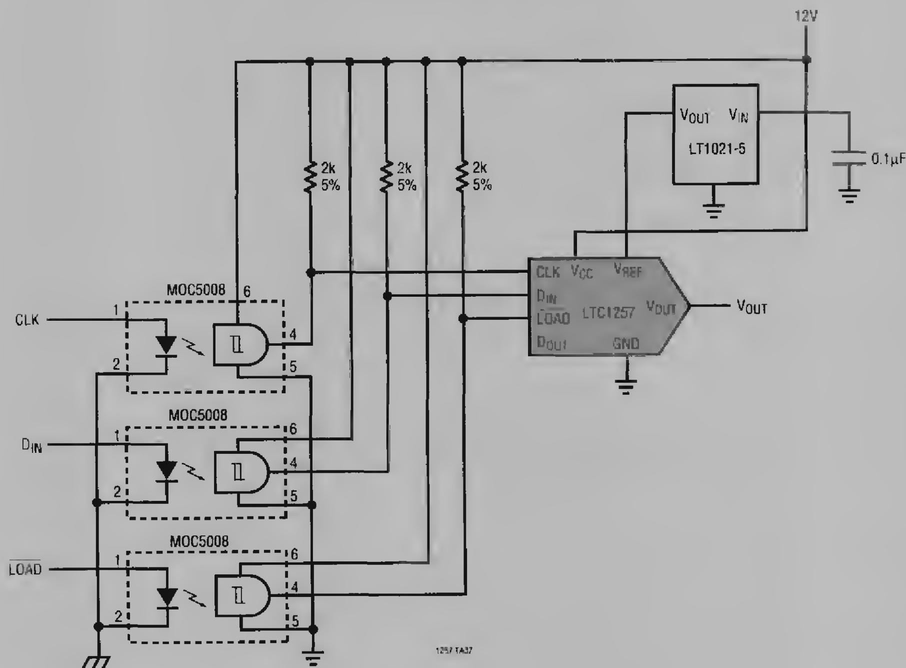


12-Bit Single 5V Control System with Shutdown



TYPICAL APPLICATIONS

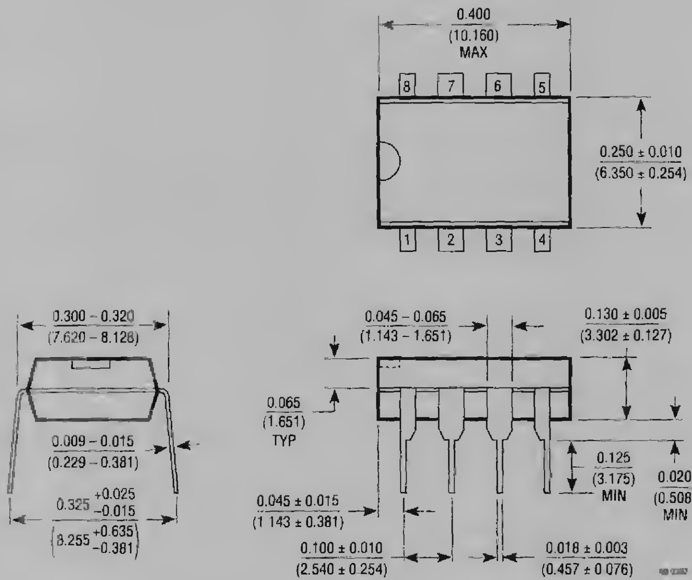
Driving LTC1257 with Opto-Isolators



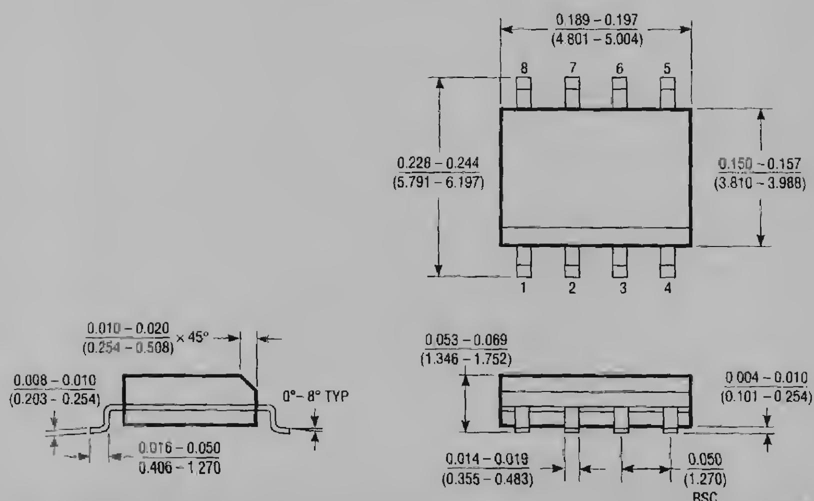
PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

N8 Package
8-Lead Plastic DIP



S8 Package
8-Lead Plastic SOIC



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